Tolerance Band Controller for a Three-Level Four-Quadrant Converter Including DC Link Balancing

Joachim Böcker
Institute of Power Electronics and Electrical Drives
University of Paderborn, Germany
boecker@lea.upb.de

***Abstract*—Tolerance band or hysteresis control is usually applied only for simple converters with one switching element. The paper shows how to generalize the approach for more complex converter systems like a three-level four-quadrant converter and to benefit from the high effective loop gain of the control approach. State graphs are used for the design of the controller. For the three-level converter, the state graph is able to manage both tasks of current control and DC link balancing. The controller can be realized using a FPGA. A processor or a microcontroller is obsolete.**

I. INTRODUCTION

Tolerance band or hysteresis control is a very powerful approach because of the high effective loop gain, which results in an excellent dynamic response and good robustness. The original hysteresis approach can easily be applied to converter control problem, if there exists *one* control objective, e.g. the current, and only *one* switching command, e.g. as with simple buck or boost converters.

More complex converters as parallel, series or multilevel topologies require the coordination of several switching commands. This is usually done by conventional controls and phase-shifted (interleaved) pulse width modulated (PWM) command signals. The so-called peak current mode control [1] is a combination of PWM and a one side threshold switching that is also able to manage interleafed switching of parallel converters, but which involves problems of instability regions.

However, though not obvious, it is possible to apply a generalized tolerance band control approach also to such complex converter structures and retain the advantages of a high control loop gain, cf. [2] [3] [4] [5] [6].

This paper shows how to design a tolerance band controller for the current control of a three-level four-quadrant converter. The concern of this paper is not only to present the particular controller as a result, which may be also found by a more ad-hoc approach, but to clearly describe the design process making use of state graphs. Designing controllers by means of state graphs seems to be a promising method also for other converter topologies.

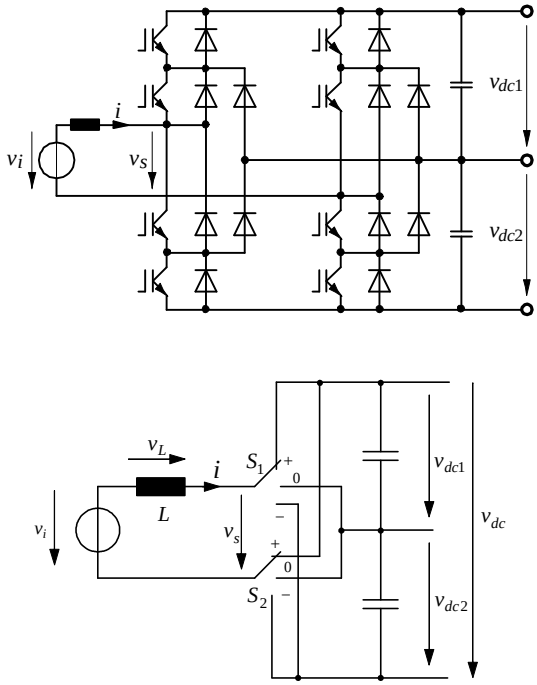

Fig. 1. Three-level four-quadrant converter and its idealized representation as a switching network

II. THREE-LEVEL FOUR-QUADRANT CONVERTER

The circuit diagram of a three-level four-quadrant converter is shown in Fig. 1. From the viewpoint of control design, the converter can be replaced by ideal switches. Each converter leg is represented by a switch with three possible switching states that are denoted as "+", "0" and "". This results in total in nine different converter states as shown in Table I.

Supposing equal DC link voltages as during normal operation, $v_{dc1} = v_{dc2} = v_{dc}/2$, five different converter voltages can be realized, which are

$$v_s = \left\{ -v_{dc},\ -\frac{v_{dc}}{2},\ 0,\ +\frac{v_{dc}}{2},\ +v_{dc} \right\}.$$

The zero voltage can be realized by three, the voltages $\pm v_{dc}/2$ by two different switching states, which are called redundant states.

TABLE I
SWITCHING STATES AND RESULTING CONVERTER VOLTAGE

S_1	S_2	v_s
–	–	0
0	0	0
+	+	0
+	0	$+v_{dc1}$
0	–	$+v_{dc2}$
–	0	$-v_{dc1}$
0	+	$-v_{dc2}$
+	–	$+v_{dc1}+v_{dc2}$
–	+	$-v_{dc1}-v_{dc2}$

III. TOLERANCE BAND CONTROL STRATEGY

The current control is usually only the inner loop of a cascaded control, which has to regulate, for example, the DC link voltage $v_{dc}=v_{dc1}+v_{dc2}$. The outer voltage controller determines the current demand i^* for the inner current control. This paper, however, focuses only on the inner current control, see Fig. 2.

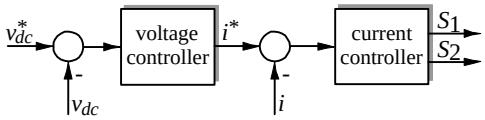

Fig. 2. Cascaded control structure

The main idea of a tolerance band current control is pretty clear: When the current hits the lower threshold of the tolerance band, the converter voltage has to be decreased, when the current hits the upper threshold, the voltage has to be increased, Fig. 3. These events of hitting the upper and lower threshold will be represented by the binary signals E_+ and E_-, respectively:

$$E_+ = \left(i > i^* + \Delta i \right)$$
$$E_- = \left(i < i^* - \Delta i \right)$$

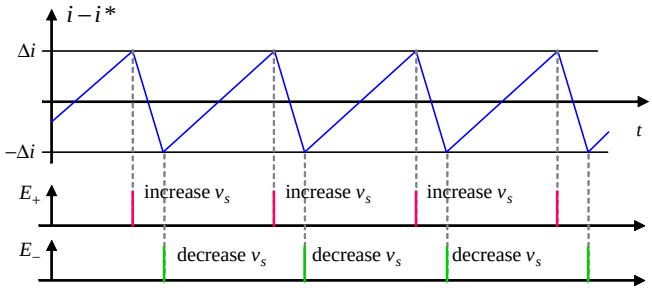

Fig. 3. Tolerance band control

However, some additional issues have to be considered:

- The switching actions should be distributed equally to the switches in order to get balanced switching losses.
- The switching actions should be used economically to reduce switching losses or to get a small current ripple, respectively.
- The DC link capacitors have to be charged equally.

The requirements can be fulfilled, if only the smallest possible driving voltages are used along the input inductance L, and, if redundant states are alternated to balance the load of the switches and the DC link. If, for example, the input voltage v_i is somewhere in the range between $v_{dc}/2$ and v_{dc}, only the converter voltages $v_s=\{+v_{dc}/2, +v_{dc}\}$ should be used to increase or decrease the current, resp., because these voltages results in smallest current slopes:

$$L\frac{di}{dt}=v_L=v_i-v_s=\begin{Bmatrix} v_i-v_{dc}/2 & >0 \\ v_i-v_{dc} & <0 \end{Bmatrix}$$

The voltage $v_s=+v_{dc}$ can be realized only by the state $(S_1,S_2)=(+-)$, so there is no choice, but the representation of $v_s=+v_{dc}/2$ should alternate between $(+\,0)$ and $(0\,-)$ for balanced load. This leads to a periodic sequence of four states, which is

$$(+-) \xrightarrow{E-} (+\,0) \xrightarrow{E+} (+-) \xrightarrow{E-} (0\,-) \xrightarrow{E+} (+-) \xrightarrow{E-} \cdots$$

If that sequence is arranged as a cycle, a state graph as shown within Fig. 4 results. The transitions between the states are triggered by the events E_+ and E_-, respectively. Such a control specification using a state graph is much clearer than a nested "if-then-else" construction of a sequentially programmed algorithm.

Another cycle can be constructed for the range $0<v_i<v_{dc}/2$. This cycle makes use of all three representations of the zero voltage, see Fig. 5. The cycles for the other two ranges $-v_{dc}/2<v_i<0$ and $-v_{dc}<v_i<-v_{dc}/2$ are similar to the presented ones, so that they are omitted here. In total, there exist four such cycles for the particular ranges of the input voltage.

The task is now to link the four separate cycles. One road could be to switch from one cycle to another by measuring the input voltage v_i. But that can also be done observing only the current control error without any voltage measurement: After a switching action, the current will usually be forced back into the tolerance band and will hit the opposite threshold next. If this is not the case, i.e. the current remains outside the tolerance band or hits the same threshold twice, it indicates that the chosen voltage is no longer sufficient and it has to be switched over to one of the adjacent cycles. For practical realization, the time delays of the system have to be taken into account so that the

procedure is as follows: A timer will be started, when the current hits a threshold (E_+ or E_-). If, after waiting an amount of time T , the same threshold is still exceeded or is hit a second time, the signals T_+ and T_- will be set. These signals are used as triggers to switch over to an adjacent cycle as shown in Fig. 6. If the opposite threshold is hit next, the timer will be reset and started again.

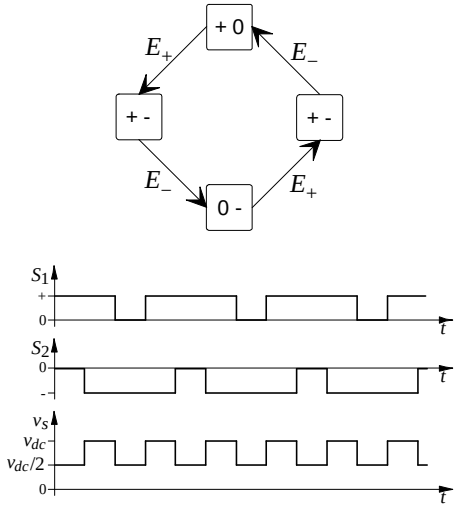

Fig. 4. Cycle for $v_{dc}/2 < v_i < v_{dc}$ and resulting switching sequence

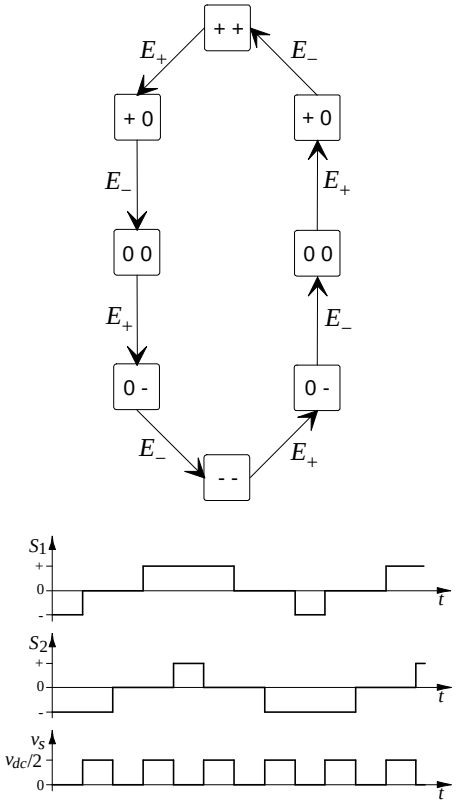

Fig. 5. Cycle for $0 < v_i < v_{dc}/2$ and resulting switching sequence

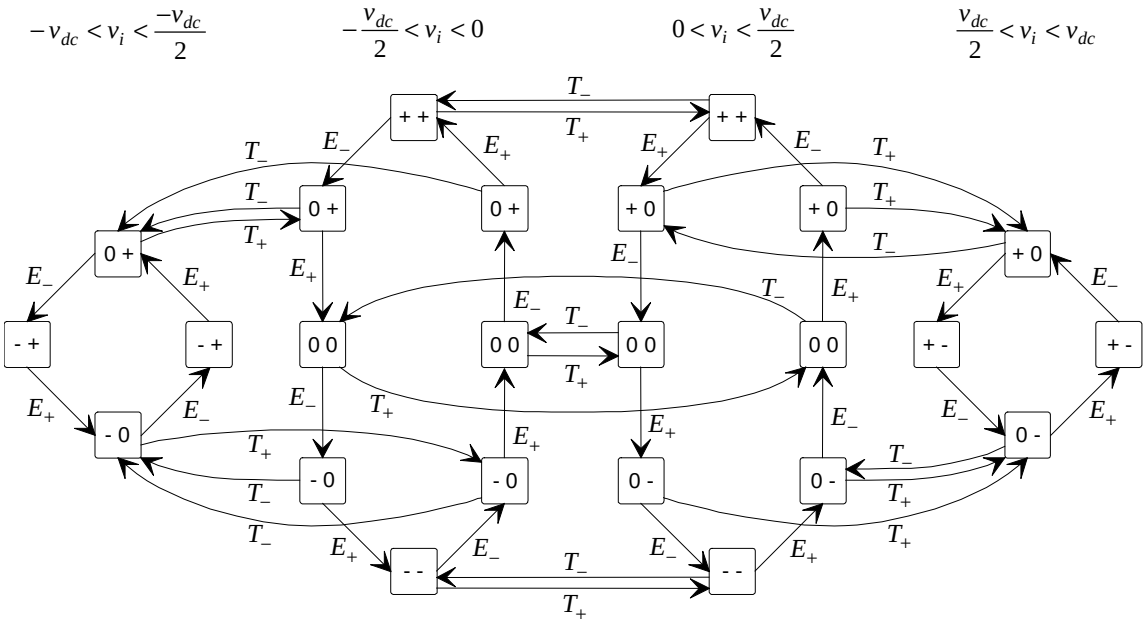

Fig. 6. Current control state graph with linked main cycles

IV. DC Link Balancing

As pointed out above, the control of the DC link voltage $v_{dc} = v_{dc1} + v_{dc2}$ is task of an outer control loop, which makes use of the demanded current i^* of the inner loop. However, it is not possible to establish an outer control that regulates both voltages v_{dc1} and v_{dc2}, because only one demand i^* is available for the inner loop. So, balancing of the voltages v_{dc1}, v_{dc2} has to be done by the inner control and must be integrated into the current controller, see Fig. 7.

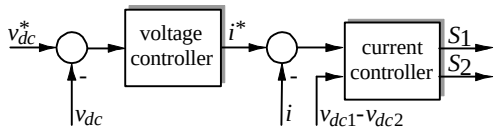

Fig. 7. Cascaded control structure with DC link balancing

The idea is to exchange the redundant states in the cycles, if the DC links are no longer balanced. Two signals are introduced to indicate that the voltage deviation is larger than an allowed threshold Δu_d. It is necessary to consider the sign of the current i for correct compensation:

$$V_+ = (v_{dc1} - v_{dc2} > \Delta v_{dc}) \wedge (i > 0) \vee (v_{dc1} - v_{dc2} < -\Delta v_{dc}) \wedge (i < 0)$$
$$V_- = (v_{dc1} - v_{dc2} > \Delta v_{dc}) \wedge (i < 0) \vee (v_{dc1} - v_{dc2} < -\Delta v_{dc}) \wedge (i > 0)$$

With these signals, the state graph is modified as shown in Fig. 8. The result is that redundant states are no longer alternated until a balanced status is reestablished. (The transitions triggered by T_m within Fig. 8 will be explained in the next section.)

V. Consideration of Minimum On/Off Time

So far, the converter was modeled as two ideal switches that can arbitrarily be switched on and off. One real effect to be considered are the minimum on and off times of the included IGBT: After switching a converter leg, a minimum time has to be passed by before successive switching is allowed without damage of the transistors. These minimum on/off time T_m is in the range of a microsecond. In most cases, no problems arise from this restriction, even if two state graph transitions are triggered within a time period shorter than T_m. The reason is that successive switchings are distributed to different converter legs so that the minimum on/off time is not violated. There are, however, some exceptions: In the case $0 < v_i < v_{dc}/2$, for example, the state graph operates in one of its inner cycles (Fig. 6). If the input voltage is assumed to be close to $v_{dc}/2$, the states that realize zero voltage (i.e. $(--)$, $(0\,0)$, $(++)$) will be activated only for very short time periods so that, e.g., the two transitions

$$(+\,0) \xrightarrow{E_-} (++) \xrightarrow{E_+} (+\,0)$$

will occur very rapidly in sequence. In that case, the transistors of the right converter leg would be turned on and off very fast in conflict with minimum on/off time. That problem can be solved by a modification of the state graph. If, e.g., the state $(+\,0)$ is held for a time longer than T_m without any external event, the following state $(++)$ will be skipped, see Fig. 8. Note that the transition is only an internal state transition, no converter switching will occur. The resulting switching sequence is then

$$(+\,0) \xrightarrow{T_m} (+\,0) \xrightarrow{E_-} (0\,0) \xrightarrow{E_+} (0\,-)\ ,$$

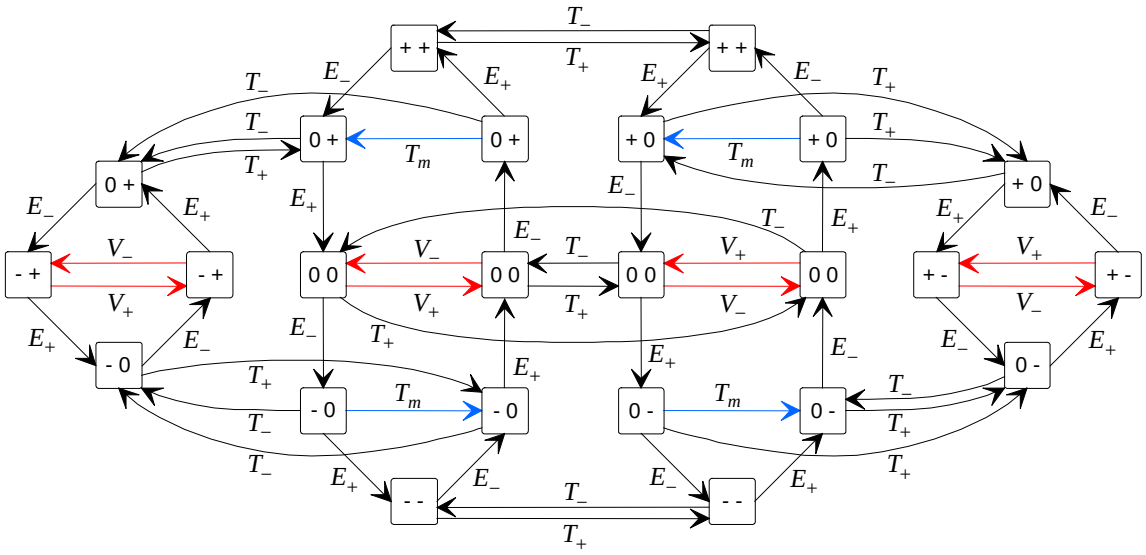

Fig. 8. Current control state graph including balancing of the DC link and consideration of minimum on/off time

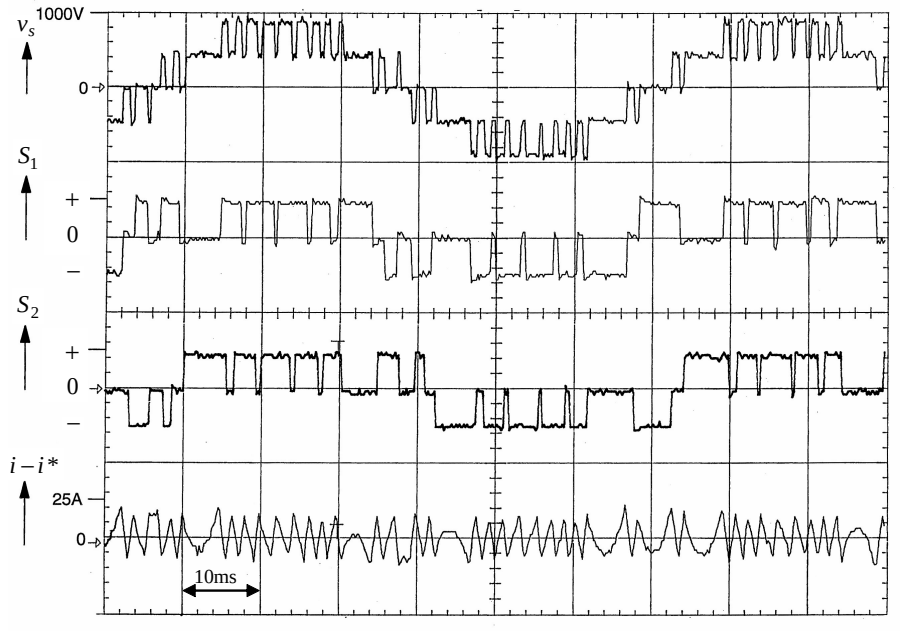

Fig. 9. Measurement result of the tolerance band control

which avoids the problem of switching the same inverter leg in rapid succession. However, it is not helpful to skip the state $(++)$ in all cases. If the input voltage is close to zero, it makes sense to use $(++)$ and $(--)$ as zero voltages to avoid other minimum on/off time restrictions in that range.

VI. Measurement Results

The controller was realized using a field programmable gate array (FPGA) with some analogue comparators. A digital signal processor or a microcontroller is not required. The controller was tested with a laboratory set up of a three-level inverter. Fig. 9 shows that the controller works well as it was designed. In particular, it can be seen from that figure, that this controller is able to cope even with a rather low switching frequency as about 100 Hz within Fig. 9, which is usually the domain of PWM approaches.

VII. Conclusion

- It has been shown how to generalize the tolerance band control method for converter systems with several switching states.
- State graphs are an appropriate method to design and to specify the controller.
- The controller can be realized using programmable logic like FPGA. A digital signal processor or a microcontroller is not necessary.
- The tolerance band control is able to manage even low switching frequencies, which are usually the domain of PWM approaches.

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