Discrete-Event Converter Control

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Abstract

Hysteresis control is a fast and robust control approach but it is mostly applied only to simple converter systems. Considering such controllers as discrete-event systems opens a more systematic view and enables the controller design even for complex converter systems like a multi-system auxiliary converter as presented here. The controller is realized without any processor only on a FPGA device.

1 Introduction

Hysteresis control is a very simple, but nonetheless, a powerful approach with excellent dynamic response and high robustness. However, for three-phase applications and more complex converter structures, pulse width modulated (PWM) controllers are predominant. The pulse width modulation allows a fixed pulse frequency and the coordination of parallel or series connected converter modules can easily be managed by phase shifts between the modulation carriers, which is difficult with hysteresis controllers. It should be mentioned that Depenbrock's [1] or Takahashi's sophisticated control strategy [2], [3] is a flux/torque hysteresis control.

The goal of this paper is to contribute to a more systematic design of hysteresis controllers from the viewpoint of discrete-event systems so that it will be possible to apply them to more complex converter topologies and to benefit from their high robustness and dynamic response.

A very interesting item is the controller hardware: Discrete-event controllers can advantageously realized on field programmable logic arrays (FPGA) with low effort.

2 The Viewpoint of Discrete-Event Dynamical Systems

The sliding mode approach is valuable for the design of the sliding surface in order to ensure convergence or stability, e.g. [6]. However, the approach does not pay much attention to a particular switching action and does not solve the coordination problem of converters consisting of parallel or series connected modules.

Considering a hysteresis controller as *discrete-event dynamical system* (DEDS) allow to focus in much more details on the switching actions and will enable a better understanding of the controller design

for more complex converters. A discrete-event system reacts only, if an event is recognized. The triggering events, e.g., of a simple hysteresis current controller are:

- $E+$: “current control error hits the upper threshold”
- $E–$: “current control error hits the lower threshold”

The task of the controller is to switch the driving voltage up or down, depending on the encountered event, in order to force the current back into the tolerance band. With a simple hysteresis, the controller output is immediately the converter firing command so that controller *state* is identical with the controller *output*, but this is not generally valid for discrete-event systems. The set of possible internal controller states may be larger than that of possible controller outputs. Distinguishing between controller output values and internal controller states is very helpful for the design of more complex systems. A simple example shall be investigated first:

3 Current Control of a Four-Quadrant Converter

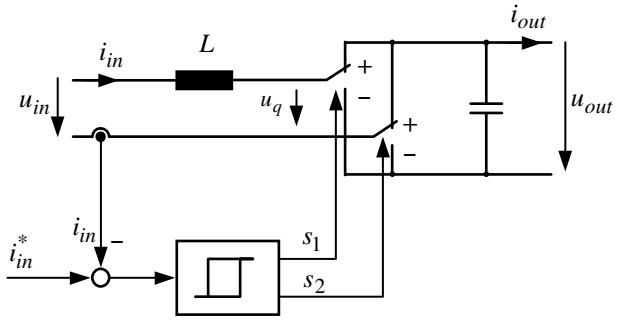

Fig. 1 Current control of a four-quadrant converter

As a starting example, a four-quadrant converter (4QC) shall be discussed (Fig. 1). The converter is fed by an AC input voltage u_{in}, the output u_{out} is a DC voltage. This discussion is focused only on the current control loop. The design of a discrete-event current controller for a 4QC is simple, but already a non-trivial task, because the switching of two converter legs have to be coordinated depending on only one control objective, cf. [4]. The converter voltage u_q depends on the converter switching states as follows:

s_1	s_2	u_q
–	–	0
–	+	$-u_{out}$
+	–	$+u_{out}$
+	+	0

The current follows the differential equation

$$L\frac{\mathrm{d}i_{in}}{\mathrm{d}t} = u_{in} - u_q \ .$$

For the controller design, some additional requirements have to be taken into account:

- Minimize the current ripple. This can be achieved by switching u_q between 0 and $+u_{out}$ in case of a positive input voltage u_{in}, and between 0 and $-u_{out}$ in case of negative u_{in}, respectively.
- Minimize the number of switching actions.
- Switching actions should be evenly distributed to both converter legs.

Having in mind that the 4 possible switching states (s_1, s_2) are only the output of the controller, not necessarily the internal controller states, will lead to a straightforward solution as it is shown as a state graph of a discrete-event controller in Fig. 2. The events *E+* and *E–* trigger the transitions between the states. The controller output (s_1, s_2) of each state is directly denoted in the state bubble.

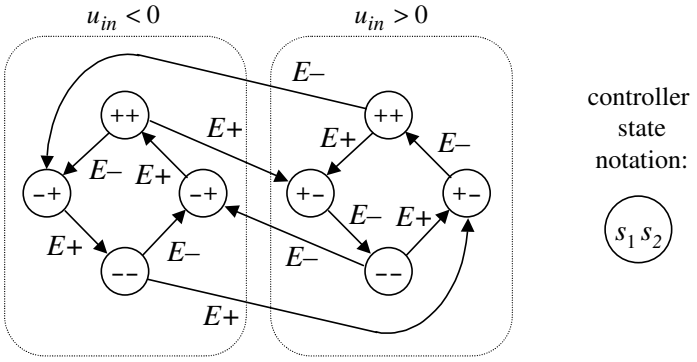

Fig. 2 State graph of the 4QC current controller

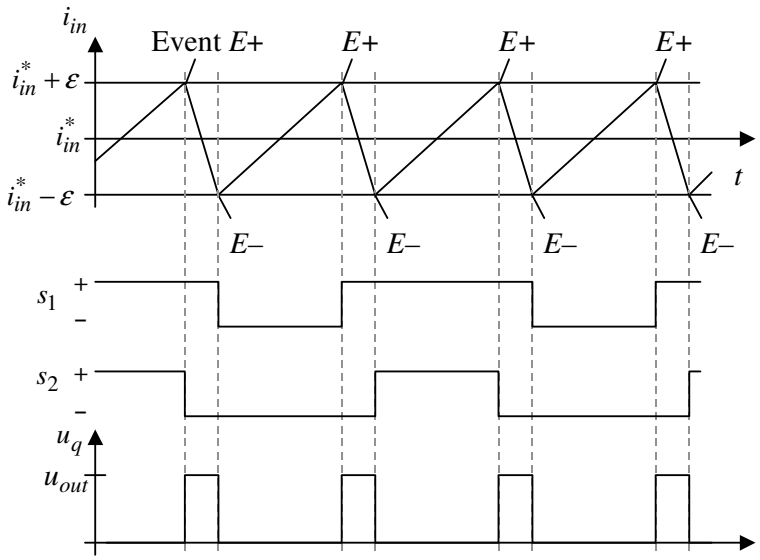

Fig. 3 Time behavior of the 4QC controller for $u_{in} > 0$

The resulting time behavior is depicted in Fig. 3. For a positive input voltage u_{in}, the active state toggles counterclockwise within the group of four states on the right side of Fig. 2. This cycle includes two controller states which are generating the same converter switching state (+,–) as output. Therefore, both zero voltage switching states (+,+) and (–,–) are applied alternatively so that the switching actions are evenly distributed to both converter legs. The converter voltage u_q toggles two times between 0 and $+u_{out}$ during one cycle, see Fig. 3. The four states on the left are used for negative u_{in} correspondingly. As mentioned above, the number of 8 internal controller states in total

is now much larger than the number of the 4 converter switching states with only 3 resulting different converter voltages.

Even though the partitioning of the state graph into the two groups for different cases of u_{in} facilitates the design, no measurement of u_{in} is, however, necessary to switch between the two groups.

A detail has to be considered for an accurate realization: After detecting an event *E*+ or *E*–, i.e. when the control error hits the upper or lower threshold, possibly following events should be suspended for a short time in order to avoid undesired switching actions due to measurement noise and time delays of the system.

4 Multi-System Auxiliary Converter

4.1 Converter System

Subject is an auxiliary converter for a railcar, which provides a constant DC output voltage u_{out} as on-board energy supply, Fig. 4. The converter can be fed directly by a DC overhead line, by the locomotive transformer in case of AC voltage systems, or by a diesel generator of the locomotive. All this results in various converter input voltages of 1, 1.5, and 3 kV, AC as well as DC. The converter consists of six modules which can be configured in various parallel or series configurations to adapt to the input voltages. Fig. 5 shows one of these configurations with two parallel branches each consisting of three modules in series. Each module (Fig. 6) includes an input rectifier, a boost converter and a DC/DC converter with galvanic decoupling, which is operated in an open-loop control mode and out of the scope of this paper. For more details see [7].

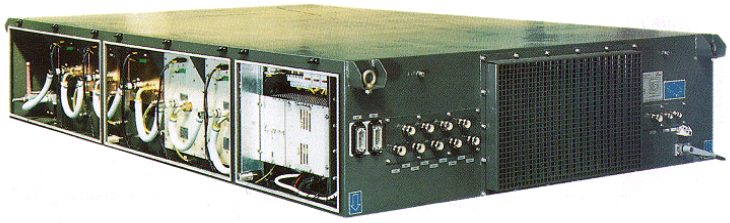

Fig. 4 Multi-system auxiliary converter for a railway application with a rated power of 100 kW

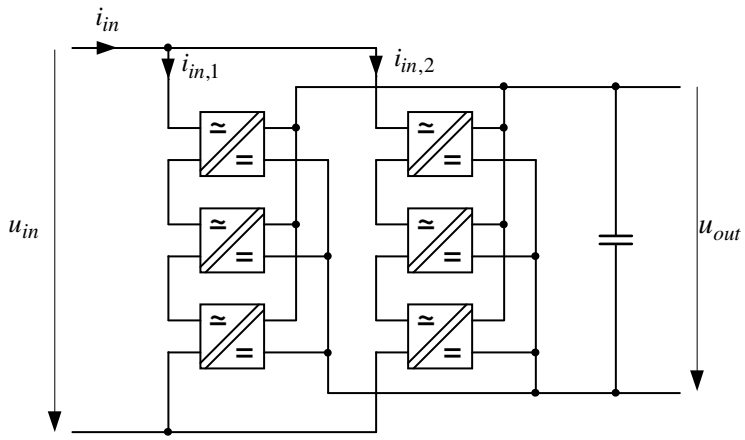

Fig. 5 Auxiliary converter in the 2×3 configuration (2 parallel branches, 3 modules in series)

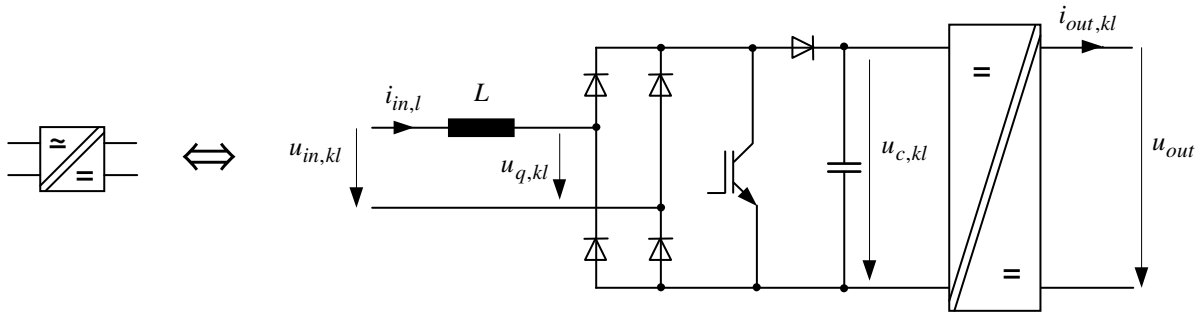

Fig. 6 Converter module *k* of branch *l*

4.2 Control Design

The primary control design goal is to keep the converter output voltage u_{out} constant, independent of the load current i_{out} and fluctuations of the input voltage u_{in}. For that purpose, a cascaded control consisting of an outer voltage control and inner PWM current control was suggested first as the parallel and series connected modules can be easily handled by phase-shifted PWM.

The control design has to pay particular attention to the input impedance

$$Z_{in}(\omega) = \frac{U_{in}(\omega)}{I_{in}(\omega)}$$

of the converter system, because the UIC specifications for railway systems are to be met [8]. The input impedance results from the complete closed-loop control behavior and cannot be determined only from the passive elements of the converter. Anyway, due to reasons of weight and volume it is not reasonable to satisfy the specification using only passive devices, in particular inductances. From the viewpoint of control design, the input impedance is the inverse of the disturbance transfer function of the current control loop: The better the disturbance suppression the higher the impedance.

A closer inspection of the PWM current control has then shown that this approach would not meet the minimum input impedance requirement, because the control loop gain was too low and could not be further increased. The gain is limited due to the computational dead time of the digital controller. The time delay is one sampling period, which is usually synchronized with the PWM pulse period if the regular sampling method is applied. Although this time delay is rather small, it is in fact one limiting factor for the achievable impedance. For example, the impedance specification could even not be met with a sampling period of 60 kHz, i.e. a sampling period of 16.7 µs, which results in a pulse frequency of 10 kHz, because six modules share the pulses, Fig. 7.

Of course, the control gain could be increased with decreasing the sampling period. Even if the processing power were not a problem, it would also result in an increased pulse frequency with rising switching losses as the major drawback.

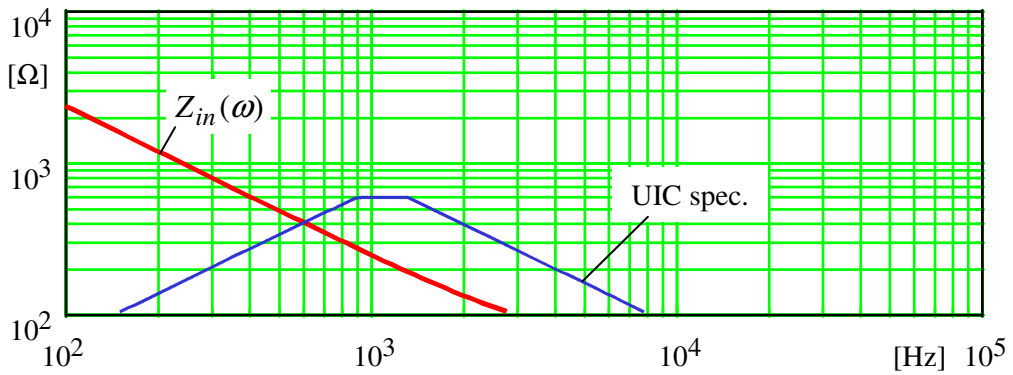

Fig. 7 Input impedances of the 2×3 configuration and PWM current control with a pulse frequency of 10 kHz and a sampling frequency of 60 kHz, compared with the UIC specification

Due to the need of such a high control loop gain, the discrete-event approach came into consideration. On a first look, the control design seems simple, because the behavior of the input current i_{in} can be described by a simplified input circuit diagram as shown in Fig. 8 with a resulting inductance

$$L' = \frac{m}{n} L$$

and an averaged converter voltage

$$u_q = \frac{1}{n} \sum_{k=1}^{m} \sum_{l=1}^{n} u_{q,kl} = \frac{1}{n} \sum_{k=1}^{m} \sum_{l=1}^{n} s_{kl}\, u_{c,kl}\, \mathrm{sgn}(i_{in,l}) \quad ,$$

where m is the number of modules in series, n is the number of paralleled branches, and $s_{kl} = \{0,1\}$ denotes the switching state of the particular module.

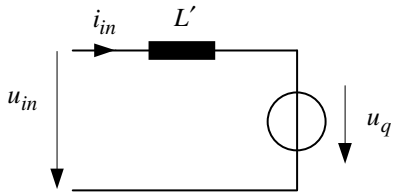

Fig. 8 Simplified input circuit of the auxiliary converter

The differential equation of the input circuit,

$$L' \frac{\mathrm{d}\, i_{in}}{\mathrm{d}\, t} = u_{in} - u_q \quad ,$$

is quite similar to that of the four-quadrant converter of Section 3, although the auxiliary converter allows only two-quadrant operation. Assuming, e.g., positive currents, then turning on a transistor (i.e. $s_{kl} = 0$) of any module will cause an increase of the time derivative of the input current, and, vice versa, turning off a transistor ($s_{kl} = 1$), will reduce the time derivative. The basic control idea is then quickly outlined:

- If the absolute current value $|i_{in}|$ hits the *upper* threshold (event *E+*), turn *off* a transistor ($s_{kl} = 1$). If the current continues to exceed the upper threshold, turn off further transistors until it comes back into the tolerance band.

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- If the absolute current value $|i_{in}|$ hits the *lower* threshold (event *E*–), turn *on* a transistor ($s_{kl} = 0$). If the current continues to exceed the lower threshold, turn on further transistors until it comes back into the tolerance band.

The problem with that control idea is that there are many degrees of freedom, because it is not clear, *which* transistor should be turned on or off. These degrees of freedom cannot be handled arbitrarily, but they must be used to take care of further objectives:

- Balancing the currents of the parallel branches $i_{in,l}$
- Even distribution of the switching actions to the converter modules

These additional requirements lead to the following more specific control strategy, which is even independent of the particular numbers of parallel branches and modules in series so that it is applicable to all converter configurations:

- In case of event *E*+ (i.e. $|i_{in}|$ hits the upper threshold)
  - select the branch *l* with the largest number of turned-*on* transistors, or, if two or more branches show the same maximum number, chose the branch with the *largest* current $|i_{in,l}|$,
  - then select within the branch *l* the module *k*, which is being turned *on* for the longest time, and turn it *off*: $s_{kl} = 1$.
- In case of event *E*– (i.e. $|i_{in}|$ hits the lower threshold)
  - select the branch *l* with the largest number of turned-*off* transistors, or, if two or more branches show the same maximum number, chose the branch with the *smallest* current $|i_{in,l}|$,
  - then select within the branch *l* the module *k*, which is being turned *off* for the longest time, and turn it *on*: $s_{kl} = 0$.

On a first look, the control strategy may possibly leave the branch currents unbalanced for some time, if the current supervision as a second-order selection criterion is applied only seldom. In reality all parallel branches will usually toggle between the same numbers of turned-on transistors, e.g. between *m* and *m*+1. So, the second-order case of a same maximum number within two or more branches will happen even every second action in average. The current balancing is therefore very effective.

Although a graphical representation of this control strategy like the state graph of the 4QC control in Fig. 2 is possible, it is getting very complex, because $2^6 = 64$ switching combinations and much more internal controller states have to be handled. Instead of this, the discrete-event control strategy was specified by an algorithm using VHDL (Very High Speed Integrated Circuit Hardware Description Language), which is more powerful than the pure graphical specification.

The switching frequency of a hysteresis controller is usually not fixed. To guarantee a specified switching frequency, a frequency controller is employed, which regulates the width of the tolerance band.

A simulation result of an AC operation is shown in Fig. 9. The supply current i_{in} follows excellently the sinusoidal shape of the demand, which is in phase with the supply voltage u_{in} (not depicted). The branch currents $i_{in,1}, i_{in,2}$ are kept balanced, but they show a larger ripple, which increases from time to time. The total current i_{in}, however, does not deviate from its sinusoidal demand at these times. Near the zero crossing of the current, the control error exceeds the tolerance band for a short time.

This is not a lack of the controller, but it is due to the two-quadrant operation of the rectifier input bridges, which are not able to provide a voltage phase advance during the zero crossing. As it can also be seen from Fig. 9, the switching actions are evenly distributed to the modules. The small variations of the tolerance band width are the reaction of the switching frequency controller.

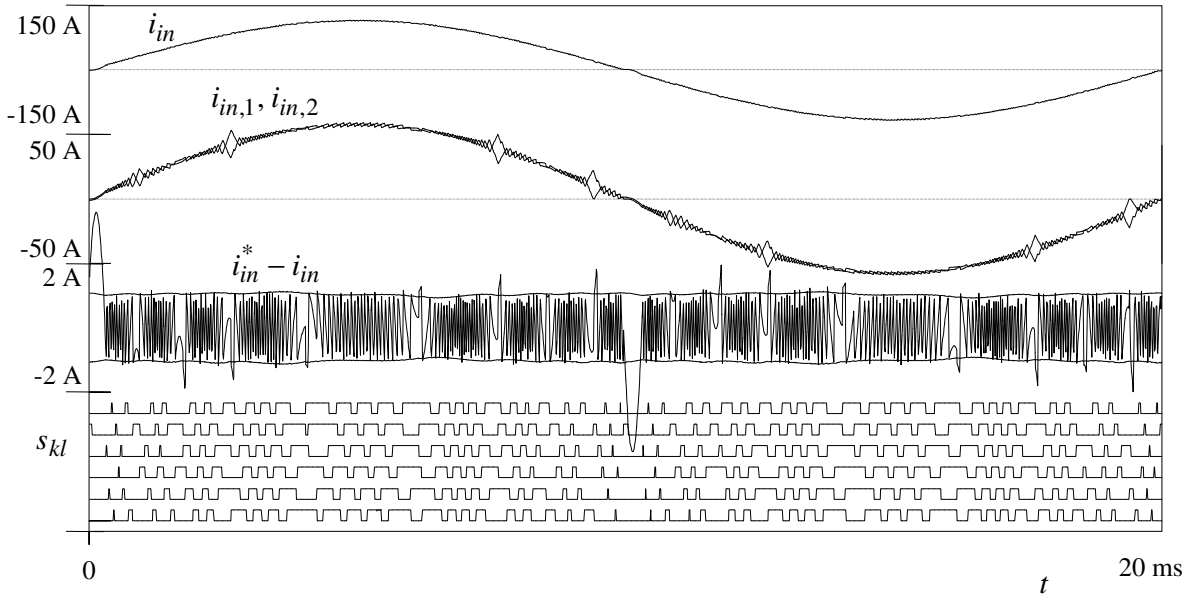

Fig. 9 Simulation result for 50 Hz AC operation of the 2×3 configuration

The control behavior of the discrete-event controller is quite satisfying, but, however, the touchstone was the crucial input impedance specification. Because the control system is now nonlinear, a quasi-impedance was numerically calculated by means of time-domain simulation. Harmonic disturbances were added to the input voltage and the response of the input current was measured. Fig. 10 shows that the controller easily meets the impedance specification due to the high effective loop gain. As a very particular result, the specification is even met with a switching frequency of only 2.5 kHz, while the PWM approach fails with 10 kHz (Fig. 7). The discrete-event control clearly outperforms the PWM approach.

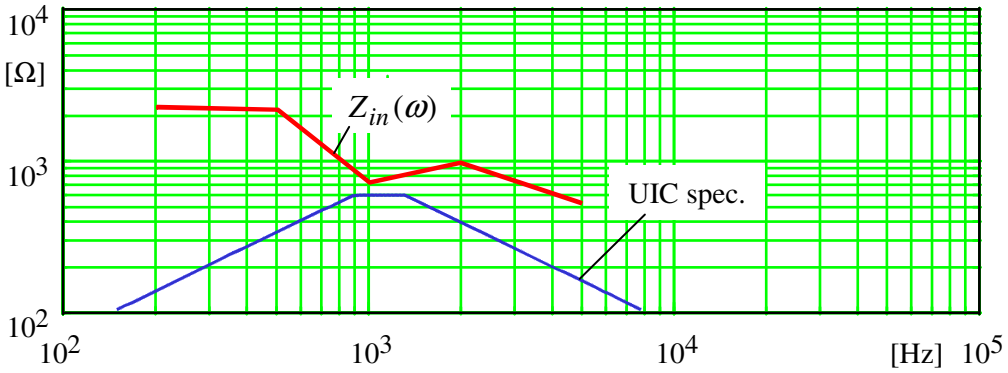

Fig. 10 Input impedances of the 2×3 configuration with discrete-event current control, compared with the UIC specification

5 Controller Hardware

A discrete-event controller should respond without noticeable time delay to an input event. For the auxiliary converter the time delay should be lower than 1 µs, which is difficult to meet with a DSP or microcontroller solution with reasonable cost. Therefore, the controller was realized using a field programmable gate array (FPGA). These logic elements can react very fast on input events and are available for low cost. The switching frequency controller and the converter protection management are also integrated into the same FPGA.

It seems that FPGA provide the natural basis for the realization of discrete-event controllers. Actually, the control board of the auxiliary converter comes only with a FPGA, without any DSP or microcontroller, Fig. 11. Some comparators are required for generating the event and condition signals from the analog measurement signals.

Observing the rapid development of FPGA, which today provides up to millions of gates on one device, even more sophisticated control tasks can be realized on this basis in the future.

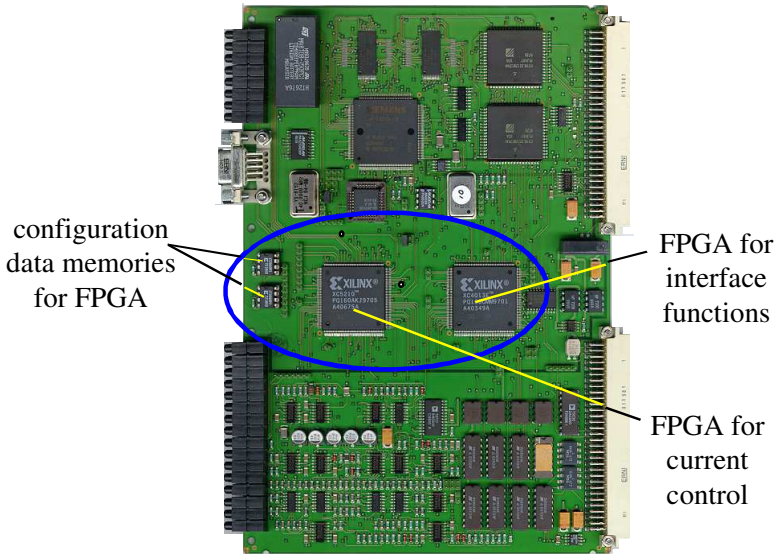

Fig. 11 Controller hardware

6 Conclusions

A discrete-event control method has been advantageously applied to a complex structure of an auxiliary converter, which requires coordinated switching of six series and parallel connected modules. The proposed method clearly outperforms the conventional PWM approach regarding pulse frequency and disturbance behavior. The discrete-event approach is able to meet an input impedance specification with a switching frequency of only 2.5 kHz, as the PWM approach even fails with 10 kHz. The controller can be realized on FPGA devices without any processor or microcontroller so that the realization effort is low. The system has been successfully proved in normal railway operation. It looks very promising to apply the control method to other converter topologies.

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